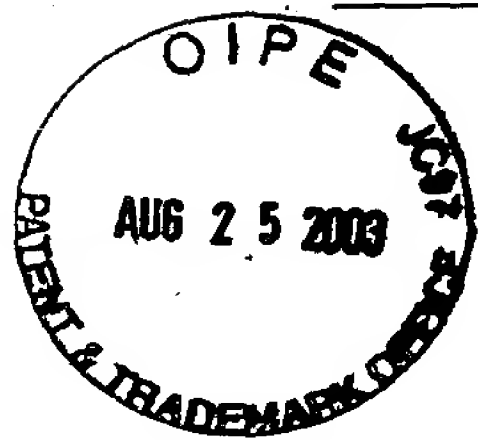


IN THE CLAIMS:



Please amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising:
a body region of a first conductivity type formed in a semiconductor substrate and having a major surface opposite to a surface shared between the semiconductor substrate and the body region;
a plurality of trench gates extending through the body region;
a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from said major surface of the body region, at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via films bordering and insulating the trench gates; ~~and~~
a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from said major surface of the body region that is less than the first depth, ~~wherein the plurality of first semiconductor regions and the plurality of second semiconductor regions are formed and defined respectively; and~~
a plurality of noncontiguous third semiconductor regions of the first conductivity type whose major extension is in a direction parallel to both the major surface of the body region and the trench gates;
wherein the body region is exposed between the plurality of second semiconductor regions and the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

2. (Previously Cancelled)

3. (Previously Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

4. (Previously Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second

semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

5. (Original) A semiconductor device according to claim 1, further comprising a wiring member connected to at least one of the plurality of trench gates.

6. (Previously Cancelled)

7. (Original) A semiconductor device according to claim 3, further comprising a wiring member connected to at least one of the plurality of trench gates.

8. (Original) A semiconductor device according to claim 4, further comprising a wiring member connected to at least one of the plurality of trench gates.

9. (Original) A semiconductor device according to claim 1, further comprising a wiring member connected to the body region and to the second semiconductor region.

10. (Previously Cancelled)

11. (Original) A semiconductor device according to claim 3, further comprising a wiring member connected to the body region and to the second semiconductor region.

12. (Original) A semiconductor device according to claim 4, further comprising a wiring member connected to the body region and to the second semiconductor region.

13. (Currently Amended) A process for producing a semiconductor device comprising:

forming a body region of a first conductivity type in a semiconductor substrate, the body region having a major surface opposite to a surface shared between the semiconductor substrate and the body region;

forming a plurality of trench gates extending through the body region;

forming a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from said major surface of the body region, at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via films bordering and insulating the trench gates;

forming a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from said major surface of the body region that is less than the first depth, wherein the plurality of first semiconductor regions and the plurality of second semiconductor regions are formed ~~and defined respectively~~ separately; and

connecting the plurality of first semiconductor regions spaced apart from one another by the second semiconductor regions;

wherein the body region is exposed between the plurality of second semiconductor regions.

14. (Previously Cancelled)

15. (Previously Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

16. (Previously Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

17. (Original) A process according to claim 13, further comprising:
forming a wiring member connected to at least one of the plurality of trench gates.

18. (Original) A process according to claim 13, further comprising:
forming a wiring member connected to the body region and to the second semiconductor region.

19. (Cancelled)

20. (Previously Added) A process according to claim 13, further comprising forming a plurality of noncontiguous third semiconductor regions of the first conductivity type whose major extension is in a direction parallel to both the major surface of the body region and the trench gates.

REMARKS

By this Supplemental Amendment, claims 1 and 13 are amended, and claim 19 is cancelled without prejudice or disclaimer, the subject matter of claim 19 incorporated into independent claim 1. No new matter is presented hereby. Claims 1, 3-5, 7-9, 11-13, 15-18 and 20 are pending. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Applicant would like to thank Examiner Mondt for the courtesies extended to Applicant's representative during the July 15, 2003 telephone interview. During the interview, Applicant's representative proposed amending claims 1 and 13, and discussed differences between the Mo et al. reference and the present application, including the features recited in claims 19 and 20.


The subject matter from claim 19 is hereby incorporated into independent claim 1, and claim 13 is amended for clarity.

In view of the foregoing, all the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

PILLSBURY WINTHROP LLP

By: 
Glenn J. Perry
Reg. No.: 28,458
Tel. No.: (703) 905-2161
Fax No.: (703) 905-2500

GJP/ASW
1600 Tysons Boulevard
McLean, VA 22102
(703) 905-2000